

Link on 8 Cavity PCB with two 10x10 Via-Arrays

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I. DESCRIPTION

The printed circuit board (PCB) provides a link between two via-arrays, as shown in Fig. 1 (a). In the first signal layer (from top of the PCB) both via-arrays are connected with striplines. Overall 12 ports are on the board. All power vias are connected with a $5\ \Omega$ resistance to the ground plane on top and bottom of the PCB. The stackup of the PCB is shown in Fig. 1 (b). The stackup has overall 8 cavities. All vias are through vias except for the signal vias with connected ports and striplines. These vias are blind vias from the top of the PCB to the first cavity with the striplines. The power vias are connected to all power planes, ground vias are connected to all ground planes.

The two top most cavities and the two bottom most cavities have fixed cavity heights, as shown in Fig. 1 (b).

II. MODELING TOOL

All simulations have been carried out with a physics-based (PB) approach [1]–[3]. A demo version of the tool can be accessed over www.tet.tuhh.de. All information regarding the setup are described in the following.

III. PARAMETER

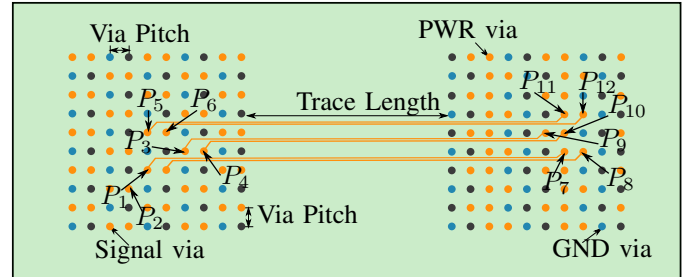
If a value is given in the tables the parameter is not altered during the simulations. On the other hand if the value is varied the according entry of the `<parameter.csv>` file is given.

A. Via Model

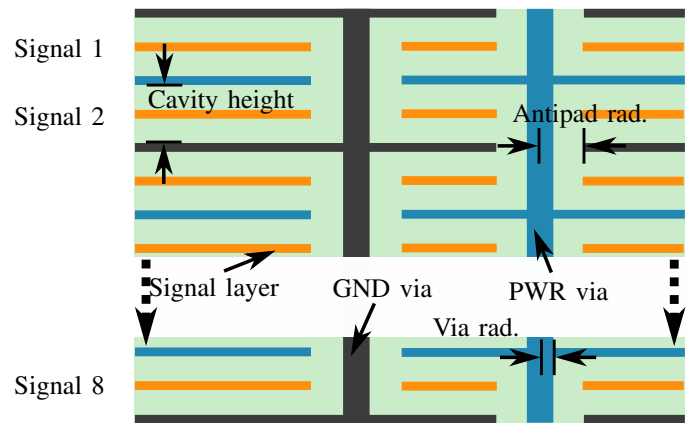
The dimensions of the vias used in the structure shown in Fig. 1 are given in Fig. 2. All vias are based on this model. For the dielectric material (Dielectric) the rel. permittivity (ϵ_r) and the loss tangent ($\tan \delta$) are given. For the conductive material (Metal) the conductivity (σ) is given. An overview is given in Tab. I.

Table I: Overview of the parameters used in the via model, as shown in Fig. 2

Parameter	Value
via radius	dc_viar
antipad radius	dc_antipadr
pad radius plane	dc_viar
pad radius signal	dc_viar



(a)



(b)

Fig. 1: (a) is the top view in the first signal layer, (b) is the stackup. GND vias are connected to all ground planes, the power vias are connected to all power planes and at the upper and lower side of the stackup the power vias are connected to the ground plane with a $5\ \Omega$ resistance. Adapted from [4]

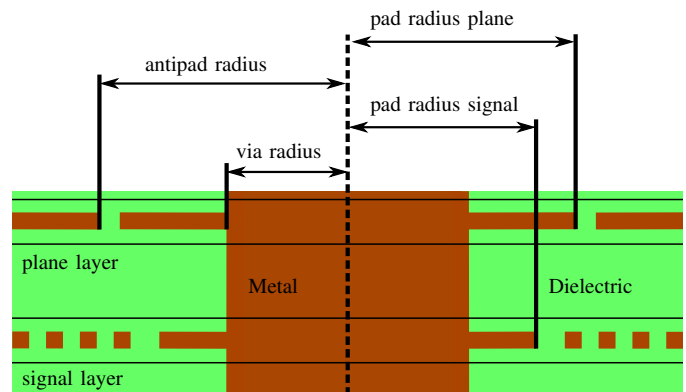


Fig. 2: Via model used for all vias of the structure. If the radius values are not given the `via_radius` is used for `pad_radius_plane`, and `pad_radius_signal`.

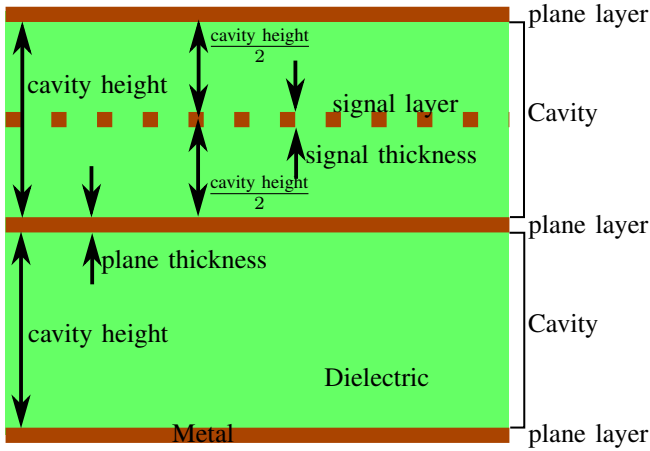


Fig. 3: Stackup nomenclature for the problem. The naming refers to all cavities unless stated differently in the description.

B. Materials

Two different materials were used, the material for the metal e.g. planes, striplines, vias, pads, and the material for the dielectric e.g. cavity filling, antipad. The metal requires two parameter conductivity (σ) and rel. permeability (μ_r). The dielectric has the rel. permittivity (ϵ_r) and the loss tangent ($\tan \delta$). An overview is given in Tab. II.

Table II: Overview of the material parameters used in the structure.

Parameter	Value
σ	5.8 S/m
μ_r	1
ϵ_r	dc_eps
$\tan \delta$	dc_tand

C. Stackup

For the stackup general parameters are introduced. If not stated differently in the description the naming refers to all cavities of the stackup. One cavity is defined by the enclosed dielectric material by two planes, as shown in Fig. 3. Signal layers are defined in the middle of the cavity. The cavity height is the distance between two plane layers (here dc_tdiel).

Table III: Overview of the parameters related to the stackup used in the PCB.

Parameter	Value
cavity height	dc_tdiel
plane thickness	1 mil
signal thickness	1 mil

D. Via Model

All striplines are in the center of a cavity. and are defined by the width and the thickness, as shown in Fig. 4. All striplines are based on this model. For the dielectric material (Dielectric) the rel. permittivity (ϵ_r) and the loss tangent ($\tan \delta$) are given.

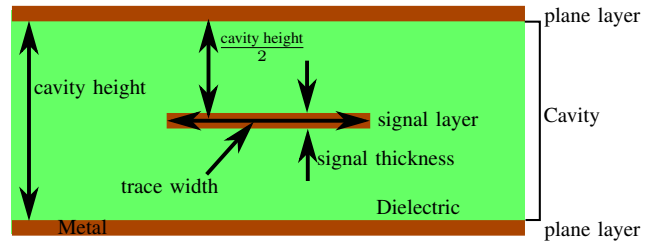


Fig. 4: Stripline model for all striplines used in the PCB.

For the conductive material (Metal) the conductivity (σ) is given. An overview is given in Tab. IV.

Table IV: Overview of the parameters used in the via model, as shown in Fig. 4

Parameter	Value
signal thickness	1 mil
trace width	dc_trace_width

E. File <parameter.csv>

The file <parameter.csv> contains all necessary information for the setup of the geometry and parameter variations. The columns are:

- index
- simuIndex
- pitch
- dc_eps
- dc_tand
- dc_viar
- dc_antipadr
- dc_tracelen
- dc_tdiel
- dc_trace_width

Index is the row in the <parameter.csv>, simuIndex is the simulation index (<index>) to find the simulation results, pitch is the via distance x-direction and y-direction inside the via-arrays, bp_eps is the the relative permittivity of the dielectric filling (ϵ_r), bp_tand is the loss tangent ($\tan(\delta)$) of the dielectric, bp_viar is the radius of each via, bp_antipadr is the antipad radius of each via, bp_tracelen is the distance between the via-arrays, bp_tdiel is the distance between two planes forming a cavity.

IV. PUBLICATIONS

This structure was used in [4]. In both publications investigations with respect to machine learning (ML) techniques were made.

REFERENCES

- [1] R. Rimolo-Donadio, X. Gu, Y. Kwark, M. Ritter, B. Archambeault, F. de Paulis, Y. Zhang, J. Fan, H.-D. Brüns, and C. Schuster, "Physics-Based Via and Trace Models for Efficient Link Simulation on Multilayer Structures Up to 40 GHz," *IEEE Transactions Microwave Theory and Techniques*, vol. 57, no. 8, pp. 2072–2083, Aug. 2009.

- [2] S. Müller, X. Duan, M. Kotzev, Y.-J. Zhang, J. Fan, X. Gu, Y. H. Kwark, R. Rimolo-Donadio, H.-D. Brüns, and C. Schuster, "Accuracy of Physics-Based Via Models for Simulation of Dense Via Arrays," *IEEE Transactions on Electromagnetic Compatibility*, vol. 54, no. 5, pp. 1125–1136, Oct. 2012. [Online]. Available: <https://doi.org/10.1109/temc.2012.2192123>
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- [4] K. Scharff, C. M. Schierholz, C. Yang, and C. Schuster, "ANN Performance for the Prediction of High-Speed Digital Interconnects and Multiple PCBs," in *Proceedings 2020 IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, California, USA, Oct. 2020.