Universal Differential SI Via Array Link with Latin Hypercube Sampling

SI/PI-Database

Institut für Theoretische Elektrotechnik

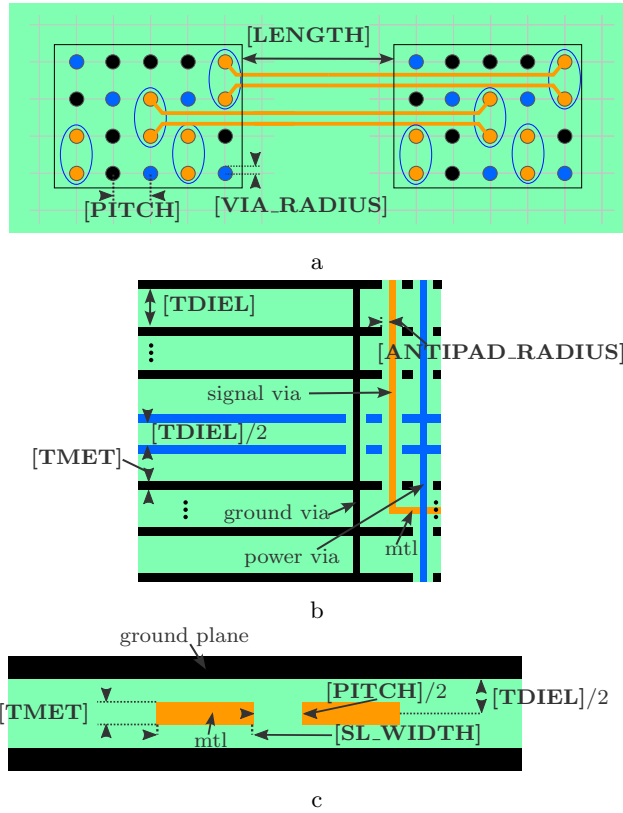Hamburg University of Technology (TUHH)

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Figure 1: a) Top view of exemplary Via array configuration, b) side view of the printed circuit board (PCB), c) front view of an exemplary Multiconductor Transmission Line (MTL). The parameters are named as found in the data files. A single Array of [**VIAS_X_AMOUNT**] × [**VIAS_Y_AMOUNT**] is defined. The array is placed on a printed circuit board (PCB) with a varied number of layers

1 Introduction

You can find all information regarding the printed circuit board (PCB) structure and setup in the following chapters. The PCB is described by the stackup, (order, type, material, thickness of layers) the board geometry (height, width), the via geometry (via radius, via antipad, etc.), the transmission lines (width, thickness, material) only if applicable and connectivity of vias, planes and [transmissions lines].

Each of the previously mentioned aspects has an individual chapter. If instead of a numerical value a variable (capitalized, bold font and square brackets) is given this parameter is varied during the electromagnetic (EM) simulations. Further information are found in Section 3.

1.1 How to Cite?

If you use the provided data you have to reference by using at least the following Open Access paper [1]:

> M. Schierholz et al., "SI/PI-Database of PCB-Based Interconnects for Machine Learning Applications," in IEEE Access, vol. 9, pp. 34423-34432, 2021, doi: 10.1109/ACCESS.2021.3061788.

This dataset was first presented in the following publication. You have also to reference this work:

> T. Hillebrecht, M. Schierholz, Y. Hassab, J, Alfert and C. Schuster, Generation And Application of a Very Large Dataset for Signal Integrity Via Array and Link Analysis," submitted for publication.

1.2 License

Please be also aware of our license agreement. You can find further information in Section 5.

1.3 Data Structure

Included in the download are multiple files and folders, see Table 1. See Fig. 1 for the parameter definitions.

Table 1: Data Directory

Name	Type	Description
<sim-title>.pdf	PDF-Document	This Description
parameter.csv	CSV Document (Delimeter = ',')	Parameter file with all parameter variations, see Section 3.
variation/	Directory	Directory containing all EM simulation results (S-Parameter), see Section 4

2 PCB Structure

The structure is a PCB with multiple planes, vias, Multiconductor Transmission Lines (MTLs) and materials. The vias, the stackup, and the MTLs are explained in the following sections. If a parameter (capitalized, bold font and square brackets) instead of a numerical value is given this parameter was changed during the EM simulation. Detailed descriptions are given in Section 3.

2.1 Board Size

The board has a rectangular shape, see Fig. 1. The dimensions are assumed to be infinitely large with the usage of a perfect matched layer (PML) boundary condition in the physics-based (PB) simulation.

2.2 Stackup

The structure has overall [**LAYER_AMOUNT**] layer, including planes, dielectrics and signal layer. The planes are modeled as solid planes over the total size of the PCB. The signal layers are assumed to be part of the surrounding cavities and are used for the potential placement of a transmission lines. The center of all stackup variations are always two power planes and two surrounding ground planes. An overview of an exemplary stackup is shown in Table 2. A detailed overview of the stackup of the respective simulation is given in the **<stackup.txt>** file.

The connectivity of a layer is used to connect corresponding vias. Dielectric Material is not connected to any net. The Material definitions are shown in Table 3.

Table 2: Printed Circuit Board Stackup

Layer	Type	Connectivity	Material	Thickness
1	plane	GND	metal	[**TMET**]
1'	dielectric	None	diel	[**TDIEL**]/**2**
2	signal	SGN	metal	[**TMET**]
2'	dielectric	None	diel	[**TDIEL**]/**2**
3	plane	GND	metal	[**TMET**]
3'	dielectric	None	diel	[**TDIEL**]/**2**
4	plane	PWR	metal	[**TMET**]
4'	dielectric	None	diel	[**TDIEL**]/**2**
5	plane	PWR	metal	[**TMET**]
5'	dielectric	None	diel	[**TDIEL**]/**2**
6	plane	GND	metal	[**TMET**]
6'	dielectric	None	diel	[**TDIEL**]/**2**
7	signal	SGN	metal	[**TMET**]
7'	dielectric	None	diel	[**TDIEL**]/**2**
8	plane	GND	metal	[**TMET**]

Table 3: Printed Circuit Board Material

Name	metal	diel
Type	conductor	dielectric
Conductivity $\sigma \left(\frac{S}{m} \right)$	[**CONDUCTIVITY**]	not applicable
Rel. Permittivity ε_r	not applicable	[**PERMITTIVITY**]
Loss Tangent	not applicable	[**LOSSTANGENT**]
Rel. Permeability μ_r	1.0	1.0

2.3   Via

The vias have multiple dimensional aspects, an overview is given in Fig. 2. The dielectric material (Dielectric) is the material from the dielectric layer, see Table 2. For each via array different via parameters are possible e.g. via radius. Additional information of the parameters can be found in the CONMLS user manual CONMLS by TET.
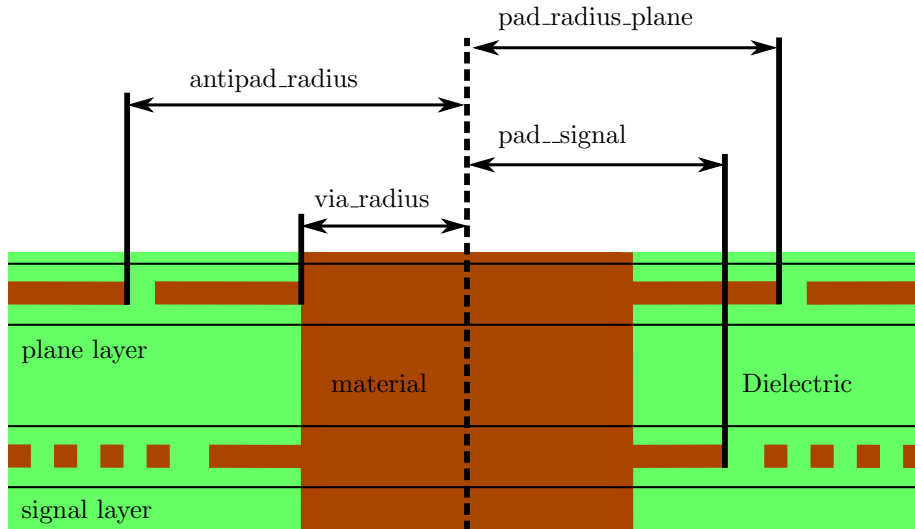
Figure 2: Overview of the via parameter e.g. via-radius. Pad radius signal and pad radius plane is relevant in the signal layer and plane layer respectively.

2.3.1 Via Model and Array

The vias of the array are organized in a block form with the amounts in x and y direction varying with [**VIAS_X_AMOUNT**] and [**VIAS_Y_AMOUNT**], respectively. Each via has a distance of [PITCH] to its neighbors. The number of vias of the three types, signal, ground and power, varies with the parameters [**SIGNAL_AMOUNT**], [**GROUND_AMOUNT**], [**POWER_AMOUNT**], respectively,see Fig. 1 a. All ground vias are connected to all ground planes. All power vias are connected to all power planes. Two signal vias are always placed adjacent to each other to enable differential signaling through post-processing. A detailed overview of the array configuration of the respective simulation is given in the <**via_array.txt**> file. The vias are labeled in the format of *via_i_j*, with i as the position in x-direction and j as the position in y-direction and *via_1_1* as the bottom left via. In this dataset always two identical arrays are placed with a distance of [**LENGTH**] between each other. The arrays are then connected using MTLs, see Section 2.3.2.

Table 4: Parameters Via Model: via_model

Parameter	Value (mil)
name	vmod
via_radius	**[VIARADIUS]**
inner_radius	0.0
pad_radius_signal	0.0
antipad_radius	**[ANTIPAD_RADIUS]**
pad_radius_plane	0.0
material	metal

2.3.2 Transmission Lines

Similar to the vias, the transmission lines also have multiple dimensional aspects, an overview is given in Fig. 3. The dielectric material is the material from the dielectric layer, see Table 2. Additional information of the parameters can be found in the CONMLS user manual CONMLS by TET.

In this dataset the MTLs are used to connect randomly selected via pairs to their counterpart of the second array. Up to four random cavities hold up to two MTLs. If a via is connected with a transmission line, it ends at the respective signal layer, leading to a back drilled via with only one wave port at the upmost layer.
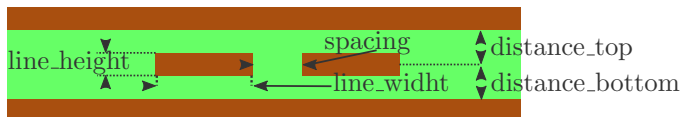

Figure 3: Overview of the MTL parameter.

Table 5: Parameter MTL

Parameter	Value (mil)
line_width	**[SL_WIDTH]**
line_height radius	**[TMET]**
distance_top	**[TDIEL]**/2
distance_bottom	**[TDIEL]**/2
spacing	**[PITCH]**/2
material	metal

3 Parameter Variation

Some parameters of the PCB are varied throughout the EM simulations. Parameters are in general marked by capital letters. All parameter variations are stored in the file **<parameter.csv>**, see Section 3.1.

3.1 Parameter Storage File <parameter.csv>

The file **<parameter.csv>** is a tabular file with multiple columns (Delimeter = ',') and rows. The first row has all the parameter names as named in the tables, figures and descriptions of this document. Each row represents one EM simulation. By the column SIMULATION the corresponding network parameters are found in the variation/ folder.

4 EM-Simulation

The EM simulations are carried out with a simulation tool developed by the Institut für Theoretische Elektrotechnik. The tool is based on physics based via and tranmission line models. In recent work of the institute many correlations with full-wave solver have been made with a high accuracy. [2–4]

The simulations are performed with PML boundary conditions. The frequency spectrum is 250 MHz to 100 GHz with 400 linearly spaced frequency points.

5   License agreement for usage of the SI/PI-Database

Institut für Theoretische Elektrotechnik, TUHH - December 2020

The SI/PI-Database is a collection of printed circuit board based structures which represent different electromagnetic aspects for signal integrity and power integrity applications. The structures have different components and interconnecting elements e.g. vias, via-arrays, power, ground planes. Each structure contains many variations with the according simulation results. All structures were simulated with a physics-based approach developed by TUHH.

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based interconnects for machine learning applications," IEEE Access, vol. 9, pp. 34 423–34 432, Feb. 2021

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6   Contact

You can find the contact information and the person in charge SI/PI-Database at TET: https://www.tet.tuhh.de/en/si-pi-database/

References

[1] M. Schierholz, A. Sanchez-Masis, A. Carmona-Cruz, X. Duan, K. Roy, C. Yang, R. Rimolo-Donadio, and C. Schuster, "SI/PI-Database of PCB-Based Interconnects for Machine Learning Applications," *IEEE Access*, vol. 9, pp. 34 423–34 432, Feb. 2021.

[2] R. Rimolo-Donadio, X. Gu, Y. Kwark, M. Ritter, B. Archambeault, F. de Paulis, Y. Zhang, J. Fan, H.-D. Brüns, and C. Schuster, "Physics-Based Via and Trace Models for Efficient Link Simulation on Multilayer Structures Up to 40 GHz," *IEEE Transactions Microwave Theory and Techniques*, vol. 57, no. 8, pp. 2072–2083, Aug. 2009.

[3] X. Duan, R. Rimolo-Donadio, H.-D. Brüns, and C. Schuster, "A Combined Method for Fast Analysis of Signal Propagation, Ground Noise, and Radiated Emission of Multilayer Printed Circuit Boards," *IEEE Transactions on Electromagnetic Compatibility*, vol. 52, no. 2, pp. 487–495, May 2010. [Online]. Available: https://doi.org/10.1109/temc.2010.2041238

[4] S. Müller, F. Happ, X. Duan, R. Rimolo-Donadio, H.-D. Bruns, and C. Schuster, "Complete Modeling of Large Via Constellations in Multilayer Printed Circuit Boards," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, no. 3, pp. 489–499, Mar. 2013. [Online]. Available: https://doi.org/10.1109/tcpmt.2012.2234211